The disclosure, abstract and drawings of this application were objected to because of certain editorial errors.

By way of this amendment, minor amendments have been made to the application to correct the editorial matters. No new matter has been added.

Enclosed herewith is a Letter to the Official Draftsperson setting forth certain amendments to the drawings that Applicants wish to make for this application. The first of these amendments is to correct the misspelling of the word "maximum" in element 3 of Figure 1. The Applicants thank the Examiner for identifying this oversight. Secondly, by way of these amendments, the Applicants have amended Figure 2 so that the row address generator 5 is depicted. As set forth in the specification, the row address generator has the same structure as the column address generator depicted in the original version of this figure.[1] The specification further describes how the row address generator carries out its operations in the same way as the column address generator.[2] It is further noted that the specification and originally filed drawings also illustrate how the comparison signal 41 generated by the row address generator comparator 4E is applied to the row address generator first adder 5B as a carry-in signal 35.[3]

New Claim 2 is directed to an address pattern generator for a digital data processing system memory that has memory elements addressable by column and row locations. The address pattern generator of this claim includes separate column and row address generators. The column address generator has an initial value register for storing an indication of a lowest column location in which data can be stored. There is a maximum value register for storing an indication of the highest column location in which the data are stored. The claimed column address generator includes

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[1] Specification page 9, lines 16-17.

[2] Specification page 10, line 27 to page 11, line 2.

[3] Specification page 10, lines 24-26 and Figure 1.

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an address register for storing a column address location. There is a first add circuit that is connected to the address register for receiving the stored column address therefrom and that is configured to produce a first incremented column address from the stored column address. The column address generator defined by Claim 2 includes a second add circuit connected to the first add circuit for receiving the first incremented address and to the initial value register for receiving the indication of the lowest column location. The claimed second add circuit is configured to produce a second incremented column address from the first incremented column address and the lowest column location. The column address generator of Claim 2 further includes a comparator that is connected to the first add circuit for receiving the first incremented column address and to the maximum value register for receiving the value representative of the highest column location. The claimed comparator is configured to assert a first comparison signal when the first incremented column address is greater than the highest column location. The column address generator recited by Claim 2 further includes a selector that is connected to the first add circuit for receiving the first incremented column address and to the second add circuit for receiving the second incremented column address and to the comparator for receiving the first comparison signal. The selector is configured to forward either the first or second incremented column address to the address register depending on the state of the first comparison signal.

The row address generator of the address pattern generator of Claim 2 includes components identical to those of the claimed column address generator. A row address generator initial value register stores an indication the lowest row location in which data can be stored. A row address generator maximum value register stores an indication of the highest row location in which data can be stored. A row address register stores a row address location. A row address first add circuit receives the stored row address from the address register and, from the stored row address, produces a first incremented row address. A row

address generator second add circuit is connected to the first add circuit for receiving the first incremented row address and to the initial value register for receiving the indication of the lowest row location and produces a second incremented row address based on these two values. A comparator is connected to the first add circuit for receiving first incremented row address and to the maximum value register for receiving the value representative of the highest row location and compares the two values and asserts a second comparison signal when the first incremented row address is greater than the highest row location. The address pattern generator row address generator of Claim 2 further includes a selector that is connected to the first add circuit for receiving the first incremented row address, to the second add circuit for receiving the second incremented row address and to the row address generator for receiving the second comparison signal and that forwards one of the incremented row addresses to the address register depending on the state of the second comparison signal.

Maruyama only discloses an address pattern generator with a number of address operating circuits 5a, 5b and 5c that are disconnected from each other. Each address operating circuit is capable of performing only a single address derivation operation such as an add operation, a subtract operation or an OR operation. The particular operation performed by the operating circuits is based on an instruction provided by the program control section 24.[4] The results of the operations performed by the individual address operating circuits are supplied to a set of output registers 6a, 6b and 6c. The output registers then selectively output one of the plurality of modified addresses over then address busses based on select signal also asserted by the program control section.[5] This arrangement does not suggest Applicants invention as recited by Claim 2 which is directed to an address pattern generator with column and row address

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[4] U.S. Patent No. 4 300 234; column 6, lines 62-68.

[5] U.S. Patent No. 4 300 234; column 7, lines 15-25.

generators that include first and second add circuits that are configured to respectively produce first and second incremented addresses and are further constructed so that the second incremented addresses are based, in part, on the first incremented addresses. Moreover, Maruyama does not suggest the feature of Applicants' claimed invention wherein the individual address generators are provided with comparators that determine which of the first and second incremented addresses are to be applied to the associated address registers.

Hart's memory system exerciser does includes a comparator that is employed to compare a calculated address to a highest memory address. However, as exemplified by his processing step block 129, the results of this comparison are used solely to determine whether or not a processing unit should continue to write data to or read data from a set of memory addresses as part of the memory testing process.[6] This system does not suggest Applicants claimed address pattern generator wherein comparators are employed to determine which one of a plurality incremented addresses should be transferred to an address register to establish the next read/write address.

The individual column and row address generators of Applicants' claimed invention have first and second add circuits that are interconnected to each other to produce first incremented addresses and second incremented addresses that are partially based on the first incremented addresses. The interconnection between the add circuits minimizes the time required to produce the second incremented addresses. Furthermore, the column and row address generators recited by Claim 2 apply either the first or second incremented addresses to the address registers immediately after it has been determined whether or not the first incremented addresses are greater than the highest preestablished column\row addresses. Thus this invention eliminates the need to spend extra processing time

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[6] U.S. Patent No. 3 751 649; column 12, lines 55-62, Figure 5b.

either calculating alternative, second, memory addresses or determining which of a plurality of incremented addresses represents the next memory location that should be accessed.

Accordingly, it is respectfully submitted that even when combined, the cited documents fail to suggest an address pattern generator having either the features or advantages of Applicants' invention as recited by Claim 2. Therefore, it is respectfully submitted that this claim is directed to a patentable invention and is in condition for allowance.

The dependent claims are all allowable at least because they depend from an allowable independent claim.

In the Office Action, U.S. Patent Nos. 4 051 460 to Yamada et al., 4 293 950, to Shimizu et al. and 4 384 348 to Nozaki were cited for allegedly being pertinent to Applicants' invention. Yamada only discloses a device for accessing a memory wherein two counter increment circuits are employed to drive separate counters that serve as the address registers; the comparator III-B internal to Yamada is used to test the output from the memory, it is not used as part of the address generation circuit.[7] Shimizu is directed to a test pattern generating apparatus that includes an address operating subsystem that is only capable of performing a single operation on an address to produce a single incremented address. Nozaki is directed to a method for testing a semiconductor memory device that employs a an address pattern generator; there is no discussion as to how particular this generator produces a specific set of addresses. Accordingly, these documents are no more relevant to Applicants claimed invention than the primary documents discussed above.

Applicants thus respectfully submit that the claims of this application are directed to an address pattern generator that is eligible for patent protection and that the claims are in an allowable form. Therefore, since the claims of this application, as well as all the parts of this application, are in an allowable

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[7] U.S. Patent No. 4 051 460; column 4, lines 58-63.

state, the Applicants courteously solicit prompt issuance of a Notice of Allowance.

Respectfully submitted,

DSG/gc

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